IN THE CLAIMS:

Please amend the claims as shown below, and cancel Claims 7, 8 and 10 without prejudice or disclaimer of subject matter. The claims, as currently pending in the application, read as follows:

1. (Currently Amended) A memory control apparatus which performs a reading operation on a memory device at a request of a plurality of masters, comprising:

read means for pre-reading data subsequent to data which any of the plurality of masters requests to read;

a prefetch buffer for holding a result of the pre-reading, said prefetch buffer storing one or more sets of information including data, an address of the data, and a flag indicating the validity of the data;

set means for setting a specific master among the plurality of masters; and

control means for determining whether or not a present master which issues a read request is the specific master set by said set means when the read request is issued from the present master, comparing a requested address with the address of data stored in said prefetch buffer, checking the flag of the data, returning the data as read data of the present master when the addresses match each other, and the flag is a valid flag, storing a result of the pre-reading in said prefetch buffer when there is no matching data and it is determined that the present master is the specific master, and refraining from changing the content of said prefetch buffer when it is determined that the present master is not the specific master.

2. (Original) The memory control apparatus according to claim 1, wherein said set means can arbitrarily set the specific master among the plurality of masters.

3. (Original) The memory control apparatus according to claim 1, wherein said apparatus is connected to the plurality of masters through a shared bus.

4. (Previously Presented) The memory control apparatus according to claim 1, wherein said read means simultaneously pre-reads data and reads data requested by the present master.

5. (Previously Presented) The memory control apparatus according to claim 1, wherein said read means simultaneously reads data requested by the present master and pre-reads data subsequent to the requested data.

6. (Original) The memory control apparatus according to claim 5, wherein said prefetch buffer stores data requested by the master and data subsequent to the requested data.

7. (Cancelled).

8. (Cancelled).

9. (Currently Amended) The memory control apparatus according to claim [[7]] 1, wherein when the present master requests a write, a requested address is compared with [[an]] the address of data stored in said prefetch buffer, and the flag is changed into a nullified state when the addresses match each other.

10. (Cancelled).

11. (Original) The memory control apparatus according to claim 1, wherein said set means can set a plurality of specific masters.